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Neuromorphic optoelectronic computing system based on semiconducting metal oxide nanocrystallites

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In pursuit of a computational system that matches the efficiency and speed of the human brain, overcoming the bottleneck of the von Neumann architecture is imperative. To this end, scientists are implementing neuromorphic computing, which emulates the biological principles of the human brain. We developed a hardware-in-the-loop neuromorphic computational block based on physical optoelectronic synaptic devices composed of ZnO, In_2O_3, WO_3, and SnO_2 nanocrystallite semiconductors. It serves to provide conductivity as synaptic plasticity. The dual optoelectronic approach of artificial synapses, in which optical signals modulate conductivity and electrical signals read it, enables the system architecture to avoid the programming (write) sneak-path currents that challenge electrically programmed memristive crossbar devices. In this proof-of-concept implementation, synaptic conductance modulation is realized physically in the optoelectronic devices, whereas leaky-integrate-and-fire neuron dynamics, thresholding, lateral inhibition, and learning-rule scheduling are implemented externally in software and microcontroller logic. The resulting hardware-in-the-loop platform is used to demonstrate device-assisted, STDP-inspired learning in a simple spike-based image-classification task. The study utilizes a fully connected, single-layer neural network with 16 input and 2 output neurons, which activate proportionally to the input data, thus classifying images.

Keywords Neuromorphic computing, Spiking neural network, Optoelectronic synaptic element, STDP, PPF

Spiking Neural Networks (SNNs) represent a new type of Artificial Neural Networks (ANNs) that more accurately mimic the behavior of biological neurons and their interactions compared to traditional ANNs[1,2]. Their training and operation are most efficient on specialized neuromorphic hardware. Such devices allow for the highest efficiency in the use of neural networks, primarily due to the mechanism of information storage and processing: all direct computations and data are localized in one place. Therefore, based on the principles of the human brain's functioning, artificial analogs - neuromorphic systems have been designed[3–5]. The hardware implementation of neuromorphic systems allows for significantly increased computational power due to the parallel processing of data across multiple computational blocks[6,7].

SNNs use the precise timing of spikes for information transmission, that is significantly different from what occurs in classical neural networks, where information encoding is achieved by representing the input vector numerically. Therefore, another approach is required to represent the input stimuli of the network[8–10]. Various procedures for transforming input data into stimuli for SNNs have been proposed, including temporal and frequency encoding[11].

During the training of a SNN, the process of changing connections or weight coefficients occurs, whereas in biological systems, synaptic connections change in a complex manner. However, as early as the 20th century, Donald Hebb[12] was able to formulate an important hypothesis, known as "Hebb's Rule". In essence, neurons that are activated simultaneously strengthen the connection between them. The training of SNNs can be divided into biologically inspired[13–19], implementing a confirmed variant of Hebbian learning: Spike-Timing Dependent Plasticity (STDP), gradient-based[20,21], and conversions from ANN, where a trained ANN is converted into SNN[22–25].

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Nowadays, there is an active transition from classical computing to artificial intelligence tasks such as big data, cloud computing, machine learning, data mining, and deep learning[26–28]. Despite significant growth in the computational capabilities of digital computers based on CMOS transistors, the von Neumann architecture has remained virtually unchanged since 1945[29] and the issue of limited bandwidth between memory and computing blocks is still relevant[30]. At the heart of neuromorphic computing is the development of an element base capable of mimicking the behavior of biological synapses and neurons. Various memristive materials have been classified according to the type of impact used to change properties: electrical, magnetic, or optical[31–38]. Memristive devices are divided into two broad classes of organic and inorganic bio-inspired hardware, which directly mimic synaptic and neuronal functions[39–41]. Moreover, a significant advantage of memristive devices is their simplified integration into integrated circuits using crossbar-array devices[42–44]. Despite significant progress in creating artificial synaptic structures, some issues remain relevant: electronic inputs/outputs limit of functional capabilities, large RC delay and power losses associated with electronic integration[45,46], and leakage currents in high-dimensional memristive crossbar architectures[47].

Optoelectronic devices attract attention due to their multitasking ability: long-term information storage, light intensity regulation, low power consumption, and absence of leakage currents. The combination of optical and electrical stimuli for synaptic-weight modulation makes optoelectronic devices attractive building blocks for synaptic arrays, although large-scale connectivity and high-throughput operation ultimately require integrated photonic sources and parallel read-out[48,49]. Additionally, since humans receive approximately 80% of information about the external world through the eyes[38], researching optoelectronic synaptic devices is important for developing visual systems. Optoelectronic synapses demonstrate not only basic synaptic functions such as STDP, Paired-Pulse Facilitation (PPF), Short-Term Plasticity (STP), Long-Term Potentiation (LTP) and Short-Term Recurrent Depression Plasticity (SRDP)[50–52], but also possess unique characteristics. For instance, synaptic plasticity depends on light wavelength, intensity, and pulse duration[53]. Multilevel optical memory is implemented using optoelectronic synaptic devices, indicating great potential in logic operations and pattern recognition[54]. Wavelength-dependent plasticity allows for color pattern recognition[55]. Optoelectronic synapses are also applicable in wireless optical communication and visual object recognition using SNN[56].

The distinctive feature of the metal-oxide optoelectronic synapses studied here is the combination of contactless optical weight modulation, electrical conductance read-out, direct storage of the synaptic state in the device conductance, and temperature-controlled tuning of retention and forgetting. This combination makes them well suited for transparent hardware-in-the-loop neuromorphic learning demonstrations and distinguishes them from purely electrically programmed synaptic devices.

In this work, we propose artificial optoelectronic synaptic elements based on semiconductor metal oxides exhibiting biologically inspired conductance dynamics. We study their synaptic functionality, including optically induced conductance modulation, short- and long-term memory effects, and temperature-controlled relaxation. These devices are then integrated into a hardware-in-the-loop neuromorphic demonstration, in which the synaptic state is physically stored in the conductance of optoelectronic devices, while the network-level operations are externally controlled. Specifically, leaky-integrate-and-fire neuron dynamics, thresholding, lateral inhibition, and STDP-inspired update scheduling are implemented in software and microcontroller logic. This framework is illustrated using a simple spike-based classification task consisting of left- and right-diagonal 4×4 patterns.

Results and discussion

Properties of synapses based on semiconducting metal oxide nanocrystallites

As artificial synaptic devices, various materials capable of emulating synaptic functions have been recently proposed[57]. In this regard, n-type semiconductor oxides have been suggested: zinc oxide (ZnO), indium oxide (In_2O_3), tungsten oxide (WO_3), and tin oxide (SnO_2). The mechanism of forming their conductivity is two-fold: the photogeneration of charge carriers (electron-hole pairs) and the adsorption/desorption of oxygen atoms and molecules in the nanocrystallites. This enables the creation of a dual optoelectronic approach, in which optical signals modulate conductivity, which is then read electrically. In addition, these devices are able to control electrical properties (conductivity) in a completely contactless manner.

In a biological sense, the function of synapses is based on the transmission of synaptic signals between neurons, beginning with the opening of ion channels. The transmission of synaptic signals between neurons starts with the opening of voltage-gated ion channels due to external impulses[58]. The diffusion of Ca^{2+} ions leads to the release of neurotransmitters from synaptic vesicles, and these ions bind to receptor sites on Na^+ linked ion channels on the postsynaptic neurons. As a result, the Na^+ gated ion channels open, allowing Na^+ to diffuse into the cell, which leads to the generation of a positively charged membrane potential. Once the membrane potential reaches the threshold, the neuron fires an action potential. This process facilitates information transmission and signal processing in the nervous system[59].

The conductivity behavior of synthesized optoelectronic synapse is shown in Figure 1. LED output with a wavelength of 395 nm serves as an analog for presynaptic impulses, and a photosensitive metal oxide semiconductor element on a conductive substrate is used as an artificial synapse. Temperature control, capable for regulating the heating of the device, is employed to modulate the properties of the synapse in analogy with neurotransmitters in biological neurons. The artificial synapse can be viewed as an optoelectronic equivalent where the optical pulse from LED resembles presynaptic input pulses and semiconducting metal oxide nanocrystallites imitate synaptic cleft response.

The transient behavior of conductivity in semiconductor metal nanocrystallites is governed by the recombination of photogenerated electron-hole pairs. Electrons are excited from the valence band to the conduction band through irradiation at the absorption edge. At room temperature, the optical band gap of ZnO corresponds to 380 nm. For single crystals of SnO_2, it is in the range from 330 nm to 355 nm, and the

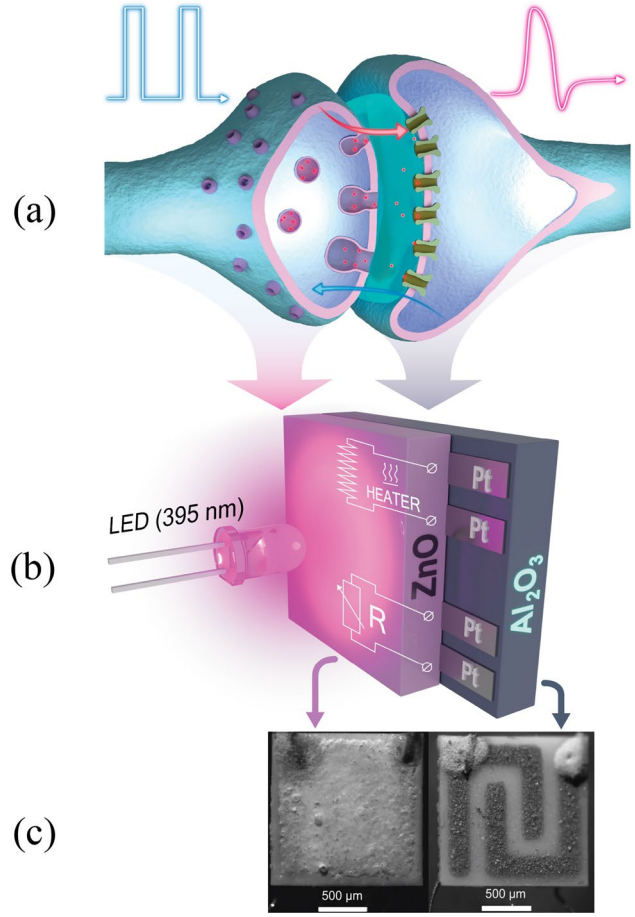


Fig. 1. The artificial synaptic device based on semiconducting metal oxide nanocrystallites: schematic diagram of the biological synapse (**a**) and artificial synapse consisting of an LED (**b**), conductive substrate and semiconducting metal oxide (**c**).

long-wavelength absorption edge of single-crystal samples of In_2O_3 is near 330 nm. The band gap for tungsten trioxide (WO_3) lies within the range of up to 410 nm. After the termination of UV irradiation, the photoinduced electrons gradually recombine back into the valence band. This process contributes significantly to the properties of short-term potentiation (short-term memory)[60]. Another process that manifests itself over a time range orders of magnitude larger than the generation of electron-hole pairs (long-term potentiation) is the absorption and desorption of oxygen atoms and molecules, which affects the conductivity properties of the material. During absorption, oxygen interacts with the surface of semiconducting metal oxides to form a chemical bond[60]. Desorption, on the other hand, is the process by which oxygen atoms or molecules are decomposed from the surface of materials, such as by heating.

To control the neuromorphic properties of semiconductor metal oxides, three heating temperatures were selected: 24°C, 100°C, and 200°C. Thus, the molecule desorption process is controlled by the thermal heating of material samples. Spiking optical pulse sequences with frequency sets ranging from 0.01 Hz to 0.5 Hz were used as a stimulus. This allowed for the investigation of the dynamic properties and responses of artificial synapses to external light exposure. A key element of the experimental study is the examination of the effects of temperature conditions on the behavior of devices, which is a necessary condition for the control process of synaptic memory. To measure the structure conductivity, an additional resistor ranging from 100 to 10^5 ohms was connected in series (the selection was based on normalizing the conductivities of all devices to a single level in complete darkness). A constant voltage of 3.3 V was applied to this system. Using an ADC, the voltage drop across the additional resistor was read and converted to conductivity. The ADC values were recorded on a PC, which also served as a control device to generate optical spikes. An LED with a wavelength of 395 nm and an average operating intensity of 3.2 mW/cm^2 was used as the presynaptic light source. Figure 2 presents the conductivity graphs of ZnO-based devices exposed to light pulses. For each temperature (24 °C, 100 °C, and 200 °C), 10 pulses were applied at frequencies of (0.01, 0.04, 0.1, 0.2, 0.3, 0.5) Hz. At 24°C, the artificial synapse exhibits a significant level of long-term synaptic plasticity, with a characteristic forgetting period that exceeds 4000 seconds. As the temperature increases, the forgetting process becomes progressively more pronounced. Within 4000 seconds, the synapse almost completely loses the information about the initial stimulus. Further temperature increase to 200°C causes the artificial synapse to relax much faster than the pulse frequency of the incident LED light. When the LED is turned off, a gradual reduction in the memory effect is observed.

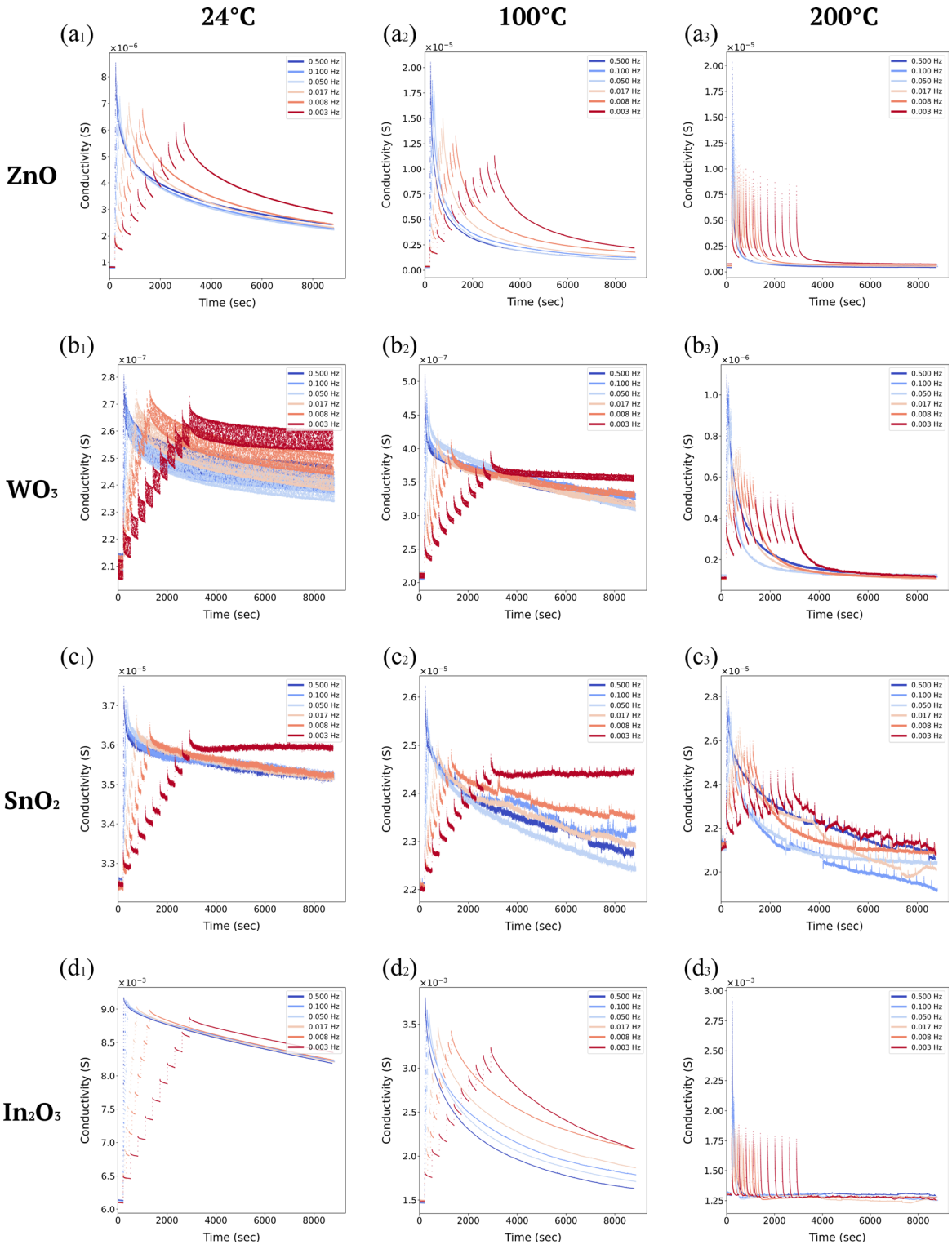


Fig. 2. The dependence conductivity on time under a sequence of light pulses at varying frequencies, measured at the temperatures of: 24°C, 100°C, 200°C. ($\mathbf{a_1}$–$\mathbf{a_3}$) ZnO oxide. ($\mathbf{b_1}$–$\mathbf{b_3}$) WO_3 oxide. ($\mathbf{c_1}$–$\mathbf{c_3}$) SnO_2 oxide. ($\mathbf{d_1}$–$\mathbf{d_3}$) In_2O_3 oxide.

This process is analogous to the decay of the excitatory postsynaptic current (EPSC) in biological systems. As a result of electron-hole pair recombination and the adsorption of oxygen atoms and molecules, the conductivity decreases to its initial level. We use temperature as an explicit control knob to tune the balance between short-term and long-term plasticity by accelerating oxygen adsorption/desorption kinetics and recombination pathways. In the array, the same effect can be implemented via micro-heaters or controlled self-heating, enabling

in-situ adjustment of retention/forgetting time without changing the optical stimulus. In our system self-control is used to accelerate device reset after training and match device time constants to the network timing budget, which directly improves training stability and inference latency.

The experimental data were also obtained for tungsten oxide (WO_3), tin oxide (SnO_2), and indium oxide (In_2O_3) synapses. For tungsten oxide, pronounced forgetting behavior is characteristic at temperatures around 200°C, whereas a lack of relaxation is observed at sufficiently high heating temperatures, approximately at 100°C. In contrast to other materials, tin oxide exhibits strong conductivity fluctuation processes when the temperature increases, even in the absence of illumination after exposure. Indium oxide is a material closely related to zinc oxide in terms of synaptic plasticity properties. Throughout the entire experimental temperature range, the device demonstrates both STM (short-term) and LTM (long-term) memory. Depending on the characteristics of the neuron and the method of activation, synaptic plasticity may manifest on either short-term or long-term time scales. Short-term plasticity reflects the history of presynaptic activity within milliseconds to minutes, while long-term plasticity represents lasting changes in synaptic strength that can persist for tens of minutes, several hours, or sometimes even days or months. Thus, the characteristics of temporal conductivity decay in nanocrystalline ZnO and In_2O_3 most closely correspond to synaptic plasticity features typical of biological systems, which led to the selection of these oxides as the basis for the development of a hardware computing system.

Paired-pulse facilitation

In a biological synapse, memory and learning occur as an analog modulation in synaptic strength resulting from presynaptic and postsynaptic activity. Neurotransmitters are released into the synaptic cleft in response to action potentials, altering the connection between presynaptic and postsynaptic neurons[61]. Paired-pulse facilitation (PPF) is one of the key properties of synaptic plasticity and occurs when a synapse is activated by two consecutive spikes with a short interval between them, where the response to the second pulse is of greater amplitude. The PPF index is defined as the ratio of the conductance after the second pulse to the conductance after the first pulse, expressed as a percentage.

The measurements of the PPF index were performed using ultraviolet illumination with a wavelength of 395 nm with 10 consecutive light pulses in the range of 1 to 300 seconds, each pulse lasting 1 second. For each semiconducting oxide, characteristic dependences of the PPF index for various temperatures were obtained, as shown in Figure 3. The obtained exponential dependences are approximated by the following function:

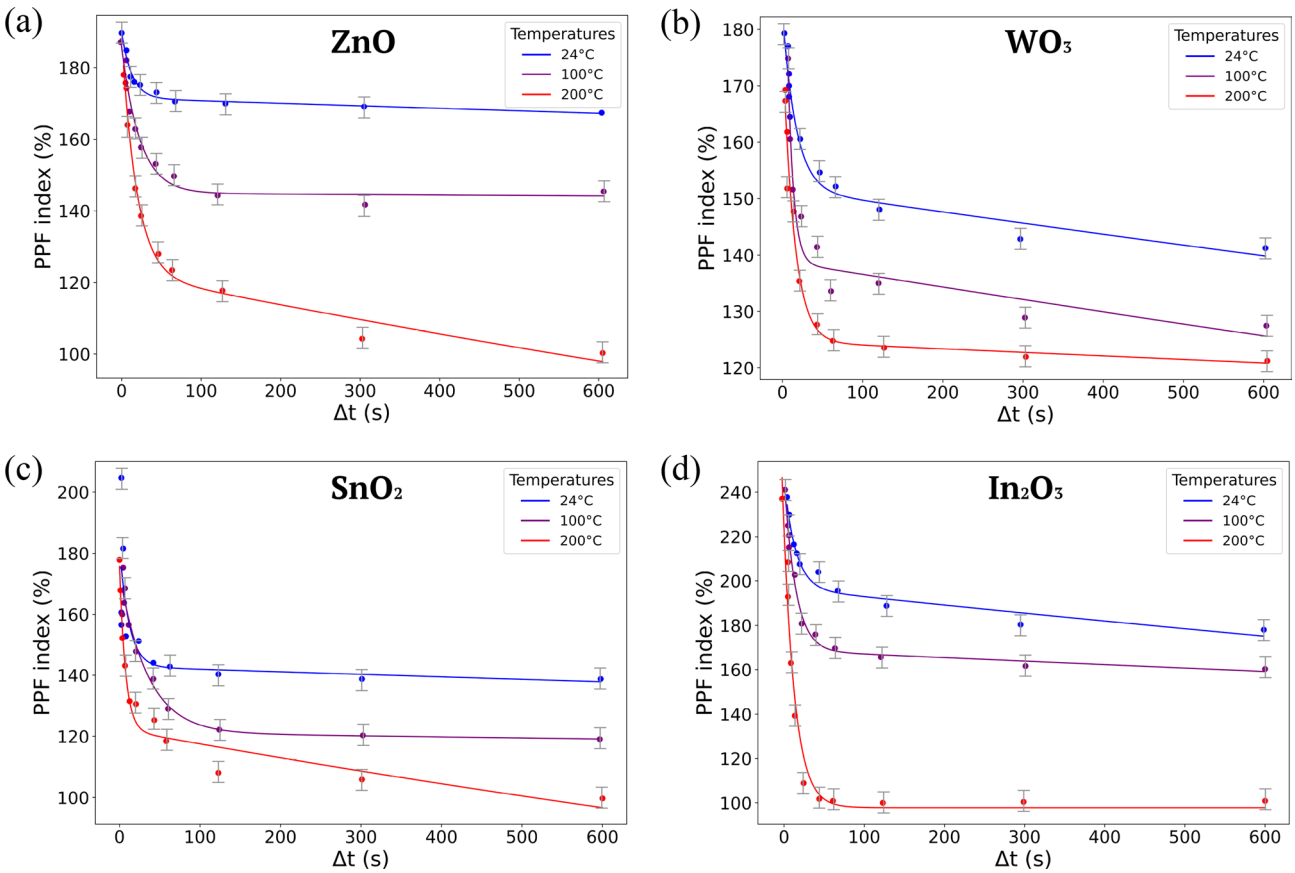


Fig. 3. PPF index for artificial synaptic devices based on (**a**) ZnO, (**b**) WO_3, (**c**) SnO_2 and (**d**) In_2O_3. Curves are PPF approximation by Eq.(1) at temperatures of 24°C, 100°C and 200°C.

$$PPF(\Delta t) = C_1 \exp\left(-\frac{\Delta t}{\tau_1}\right) + C_2 \exp\left(-\frac{\Delta t}{\tau_2}\right), \tag{1}$$

where Δt denotes the time between two sequential spikes and τ_1, τ_2, C_1, C_2 are adjustable parameters. By controlling the temperature, mechanisms were identified that govern the transition from long-term to short-term synaptic plasticity. This capability enables the adaptation of devices to accommodate learning tasks under various neural network parameters. We utilized a well-known biological learning method is applied for SNNs - STDP, which is an experimentally validated version of Hebbian learning. The STDP rule is presented as follows: suppose t_{pre} and t_{post} are the times at which the pre- and postsynaptic spikes occur, respectively. The change in synaptic weight is a function of the time difference $\Delta t = |t_{post} - t_{pre}|$. All synaptic connections that contribute to the excitation of the postsynaptic neuron should increase. Synapses that do not contribute to the excitation of the postsynaptic neuron should decrease in weight. The rule of updating weighting coefficients based on a pair of pulses is expressed as follows:

$$\Delta w_+ = C_1 \exp\left(-|\Delta t|/\tau_1\right) + C_2 \exp\left(-|\Delta t|/\tau_2\right), \quad \text{for} \quad t_{\text{pre}} < t_{\text{post}} \tag{2}$$

$$\Delta w_- = C_1^{'} \exp\left(-|\Delta t|/\tau_1^{'}\right) + C_2^{'} \exp\left(-|\Delta t|/\tau_2^{'}\right), \quad \text{for} \quad t_{\text{pre}} > t_{\text{post}}\,. \tag{3}$$

In this context, the firing rate of presynaptic neurons correlates with the intensity of incoming signals. The frequency of light impulses transmitted to the postsynaptic neuron is determined by the strength of the synaptic connection. If the membrane potential of the postsynaptic neuron exceeds a certain threshold, an action potential is generated. At this moment, it is necessary to monitor all presynaptic neurons that fired spikes immediately prior to the postsynaptic neuron and accordingly increase their synaptic weights. The weight change is based on the PPF index approximation of a zinc oxide nanocrystallite, which is considered as an optimal candidate for implementing learning processes due to its facile reconfiguration of the transition from long-term to short-term memory upon temperature increase. This dynamic adjustment of memory states via thermal modulation is crucial for developing more efficient and adaptable synaptic emulation. Additionally, the unique properties of zinc oxide nanocrystals, such as their reactivity and stability under varying thermal conditions, make them particularly suitable for simulating synaptic functions that rely on precise control of memory transition mechanisms. The weight change is taken from the PPF approximation of zinc oxide nanocrystallite as shown in Figure 3. The positive part of the weight change in Eq.(2) is based on the curve corresponding to the experiment at 24°C. The parameters of the model are taken as $C_1 = 171,\ \tau_1 = 23968,\ C_2 = 19,\ \tau_2 = 13$. Direct control of the conductivity reduction, except for temperature and the time for the devices to relax to the initial value, is not supported by the designed devices. Thus, we proposed a temporal relaxation method to control the conductance reduction. In the case where the weights are increased during training, the positive curve is modeled by the response properties of the devices when pulses are applied sequentially through the LEDs, which are characteristic of the input pulses of a spiking neural network. In the other case, when STDP should decrease the weighting coefficients, a negative curve in Figure 4 is used and controlled by temperature properties and waiting time to achieve relaxation of the devices. Consequently, the parameters for Eq.(3) are taken similarly $C_1^{'} = C_1,\ C_2^{'} = C_2,\ \tau_1^{'} = \tau_1,\ \tau_2^{'} = \tau_2$.

We emphasize that this realization corresponds to a device-assisted, STDP-inspired learning rule rather than to a fully autonomous, device-level STDP. The positive (potentiation) branch is implemented physically

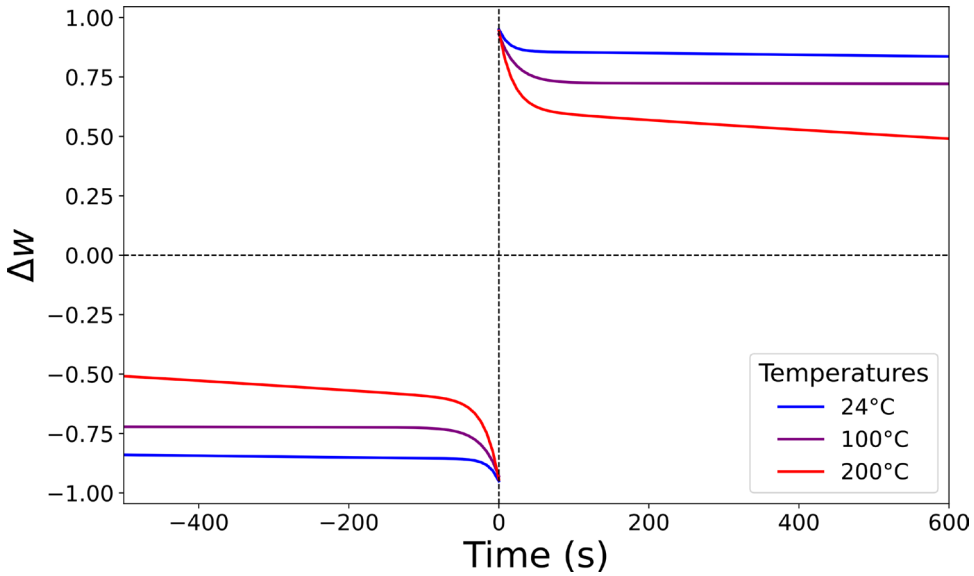


Fig. 4. ZnO-based STDP approximation curves at different temperatures: 24°C, 100°C and 200°C.

through the optically induced conductance increase of the devices, whereas the negative (depression) branch is implemented through the intrinsic conductance relaxation, accelerated when required by temperature-controlled reset. The pre- and postsynaptic spike timing and the resulting weight-update decision are computed externally in the control software; in particular, Eqs.(2)–(3) specify the magnitude of the weight change, whereas its sign (potentiation for $t_{pre} < t_{post}$, depression for $t_{pre} > t_{post}$) is assigned externally from the order of the pre- and postsynaptic spikes. A limitation of this relaxation-based depression is that it does not perform local, postsynaptically triggered coincidence detection: its rate is set by the physical relaxation and thermal time constants rather than by an instantaneous postsynaptic event, which constrains the achievable update speed and the independence of per-synapse depression. Achieving fast, per-synapse, postsynaptically triggered depression would require an additional active-reset mechanism, which we identify as a direction for future work.

To enable comparison with other analog synaptic devices, we summarize standard quantitative metrics of the plasticity derived from the measured conductance traces. The dynamic range is defined as the ratio $G_{\max}/G_{\min}$ between the fully potentiated and the baseline conductance states. The potentiation characteristic is sublinear and saturating, reflecting photoconductive charging; its nonlinearity can be quantified as the maximum deviation of the normalized conductance-versus-pulse-number curve from a linear response. Potentiation and depression are intrinsically asymmetric, because potentiation is driven by per-pulse optical stimulation whereas depression follows the bi-exponential relaxation of Eq.(1) with time constants $\tau_1 \approx 2.4 \times 10^4$ s and $\tau_2 \approx 13$ s for ZnO at 24°C. The effective update granularity is given by the number of distinguishable conductance levels resolvable within the dynamic range. These metrics place the present devices in the slow-but-high-retention regime among analog synaptic devices.

STDP curves for ZnO at different temperatures are shown in Figure 4. The final weight after each iteration is given by an expression:

$$w_{new} = \begin{cases} w_{old} + \eta \Delta w (w_{max} - w_{old}), & \text{if } \Delta w > 0 \\ w_{old} + \eta \Delta w (w_{old} - w_{min}), & \text{if } \Delta w < 0, \end{cases} \tag{4}$$

where η is the learning rate controlling the rate of the weight adaptation. To ensure that synaptic weights do not become extremely large and negative, we must consider a boundary condition for the linkage weight such that $w_{min} < w < w_{max}$. In our model, $\eta = 0.5$, $w_{min} = 0$, $w_{max} = 1$.

Image classification

The interest in the creation of learning systems based on neuromorphic properties comes from a number of advantages that SNNs exhibit over traditional ANNs[62]. SNNs, inspired by the structure and function of the biological brain, are highly energy-efficient, making them attractive for implementation in mobile devices and embedded systems. Unlike ANNs, which process information continuously, SNNs use an event-driven approach, activating only when new data arrive. This significantly reduces power consumption and increases processing speed. Moreover, SNNs can efficiently process information encoded as time sequences, that opens new opportunities in time-series analysis tasks such as speech recognition and video processing. The combination of hardware compatibility with neuromorphic chips and the high biological plausibility of SNNs opens the possibility of creating artificial intelligence systems that approximate the principles of the brain. We utilized the simplest SNN architecture for image recognition, demonstrating the feasibility of using the proposed optoelectronic synaptic block in a hardware-in-the-loop configuration for a transparent, highly specialized task based on the STDP-inspired properties of the synthesized devices.

SNN is trained using a reduced dataset of graphical images of diagonal lines created from black and white pixels. This dataset serves as input for the subsequent classification task. The training process is oriented to enable the system to efficiently identify and classify new examples based on the pre-trained models. The input images for the network are two images of diagonal lines. Each image has a size of 4x4 pixels. The spiking neural network architecture adopted for these classification tasks utilized a single fully-connected layer, is chosen for its simplicity[63]. The input image is represented as a matrix where the value of each element is proportional to the pixel intensity, and it is then fed into the neural network as a sequence of individual spikes to the first layer. Due to the incompatibility of the input signal representation with our spiking neural network, it is necessary to encode the input image into a spike sequence format. In this context, the spike impulses frequency correlates with the intensity of the pixels in the input image. The approach of information representation, where the data semantics is conveyed through the firing frequency of a pre-neuron, is referred to as rate coding. The average spike frequency of biological retinal neurons ranges from 1 to 200 Hz[64], thus scaling is performed accordingly. A pixel with maximum intensity (white) is encoded by the maximum spike frequency of 200 Hz, while a black pixel generates a pre-neuron spike frequency of 0 Hz.

To make the image-classification procedure explicit, the full processing pipeline used in the hardware-in-the-loop experiment is as follows. First, each 4×4 binary image is converted into 16 presynaptic spike trains by rate coding: white pixels generate spike trains with a higher firing probability, whereas black pixels remain silent. These spike trains are then converted by the microcontroller into optical pulses applied to the corresponding LEDs. Each LED illuminates its associated optoelectronic synaptic device, whose conductance represents the synaptic weight between one input pixel and one output neuron. The conductance state is read electrically and used by the externally simulated leaky-integrate-and-fire output neurons to compute membrane-potential dynamics and determine which output neuron fires first.

In the cerebral cortex, the timing of consecutive action potentials is highly irregular. The interpretation of this irregularity has led to two distinct perspectives on cortical organization. On the one hand, the irregularity may arise due to stochastic processes. If this is the case, the irregular interspike interval reflects a random process, implying that the instantaneous spike rate can be estimated by averaging the combined responses of many

individual neurons. According to this approach, one can expect that the precise timing of individual spikes carries little information and may lead to overfitting in a spiking neural network (output neurons spike only in groups). The Poisson process is one of the simplest models for describing the sequence of presynaptic inputs. In this case, it is assumed that the incoming impulses follow Poisson statistics. By definition, for a Poisson process with rate λ, the probability of finding an event in a sufficiently small time interval Δt is given by: $P(N = 1) = \lambda \Delta t$. Therefore, we generate a uniformly distributed random variable $r \in [0, 1]$ and trigger a Poisson event when $r < \lambda \Delta t$. This method enables the generation of Poisson-distributed spike impulses in real time.

During one training presentation, the encoded input spikes are delivered to the 16 input channels and projected to the two output neurons through the corresponding optoelectronic synapses. For each output neuron, the input current is calculated from the measured or experimentally calibrated synaptic conductances and the incoming spike events. The membrane potential is then updated according to the LIF model. When one output neuron reaches the firing threshold, it emits a postsynaptic spike and suppresses the competing output neuron through lateral inhibition. The synapses that contributed to the winning postsynaptic response are potentiated by optical stimulation, whereas synapses that should be weakened according to the STDP-inspired rule are updated through controlled relaxation of the device conductance. Thus, the physical devices provide the synaptic conductance states, while spike generation, inhibition, and update scheduling are controlled by the external hardware-in-the-loop system.

Architecture of the fully-connected spiking neural network consisting of the encoding layer and the inhibitor layer is shown schematically in Figure 5. The encoded spikes are fed into the neural network. Initially, all weights are sampled from a uniform distribution in the range [0.1, 0.3]. Each output neuron sums the incoming signals with the corresponding weight coefficients and calculates the membrane potential based on the simplified leaky integrate-and-fire (LIF) model[65]. When the threshold is reached, the output neuron generates a spike. Subsequently, the weights are updated according to the STDP-inspired rule (Eq. 4). An increase in weights corresponds to LED stimuli, while a decrease in weights reflects time delays based on STDP parameters.

It should be emphasized that the present implementation is a hardware-in-the-loop demonstration rather than a fully hardware spiking neural network. The optoelectronic devices physically implement the synaptic conductance states: optical LED pulses increase the conductance, the conductance state stores the synaptic weight, and electrical readout is used to measure this state. In contrast, the leaky-integrate-and-fire neuron dynamics, spike thresholding, lateral inhibition between output neurons, and scheduling of the STDP-inspired update rule are implemented externally in the control software and microcontroller logic.

A single training iteration is summarised as a block diagram in Figure 6 and proceeds as follows: (i) the host PC converts the current 4×4 image into 16 rate-coded Poisson spike trains, in which white pixels generate high-frequency spikes and black pixels remain silent; (ii) the microcontroller drives the corresponding LEDs, whose optical pulses increase the conductance of the addressed optoelectronic synapses; (iii) the device conductances are read electrically through the series resistor and ADC and returned to the host PC as the current synaptic weights; (iv) the PC integrates the LIF membrane potentials, and the first output neuron to reach the threshold triggers winner-take-all lateral inhibition; (v) the STDP-inspired weight update is computed from the pre- and postsynaptic spike timing and enacted on the hardware as optical potentiation (positive branch) or as scheduled relaxation/temperature-assisted reset (negative branch). This loop is repeated over the randomly presented patterns until the weight maps stabilize. In the present setup the cycle time is dominated by the device physics: the optical write uses second-scale pulses, whereas the software computations and the per-device electrical readout take of the order of milliseconds.

The model describing the dynamics of the membrane potential is as follows:

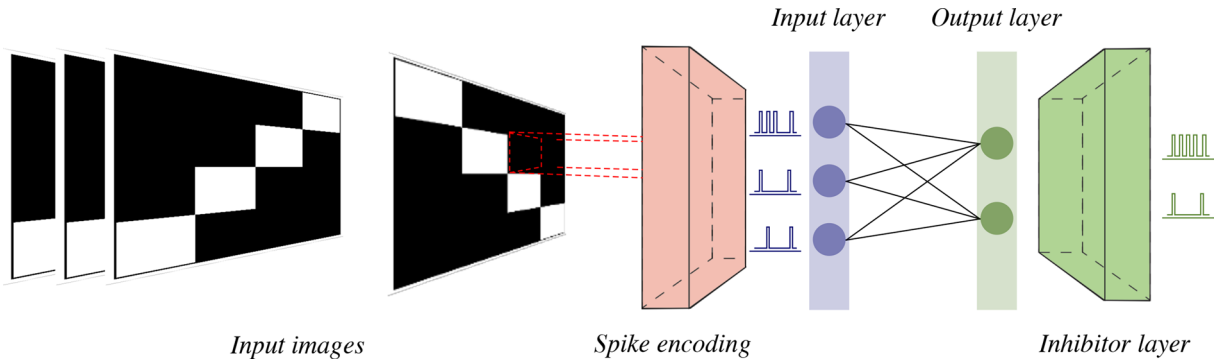


Fig. 5. System-level workflow of the hardware-in-the-loop image-classification experiment. A 4×4 binary input image is first converted into 16 rate-coded presynaptic spike trains. The generated spikes are applied to the corresponding LEDs, which optically stimulate the associated optoelectronic synaptic devices. The conductance of each device represents the synaptic weight connecting one input pixel to an output neuron. The conductance states are read electrically and used in the externally simulated leaky-integrate-and-fire output layer. When one output neuron reaches the firing threshold, lateral inhibition suppresses the competing neuron, implementing a winner-take-all learning mechanism.

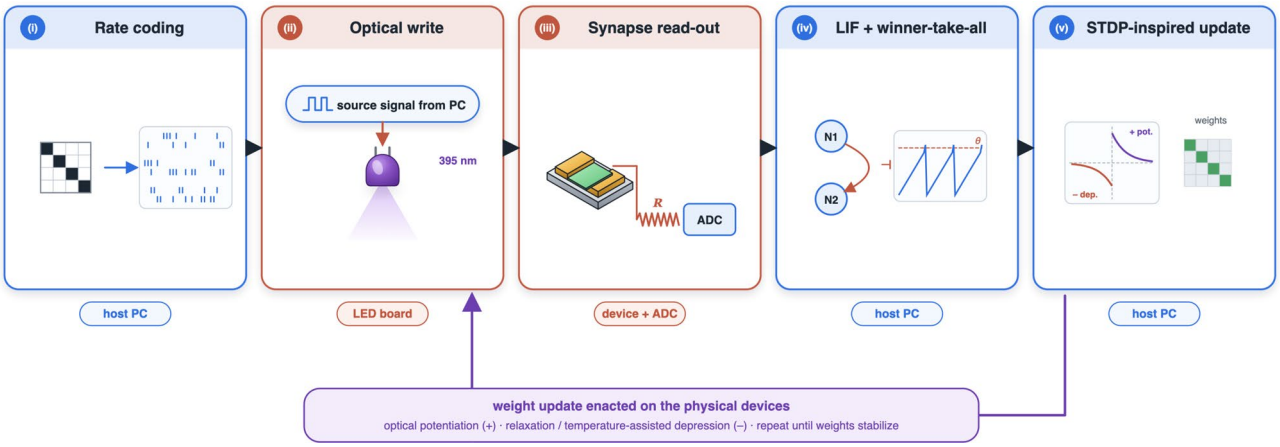


Fig. 6. Block diagram of a single hardware-in-the-loop training iteration. Blue blocks are executed on the host PC (software); salmon blocks are performed by the physical hardware. (i) rate coding of the 4×4 image into 16 Poisson spike trains; (ii) optical write, in which the host-PC source signal drives the 395 nm LED board that potentiates the addressed synapses; (iii) electrical read-out of the device conductance, i.e. the synaptic weight, through a series resistor and ADC; (iv) leaky-integrate-and-fire integration with winner-take-all lateral inhibition; (v) STDP-inspired weight update (potentiation/depression) enacted on the devices, repeated until the weight maps stabilise.

$$RC\frac{du}{dt} = -[u(t) - u_{rest}] + RI(t), \tag{5}$$

where R is membrane resistance, C is membrane capacity, u is membrane potential, I is input current and u_{rest} is resting membrane potential. As the membrane potential reaches the threshold value, the potential sharply increases, and the neuron enters a refractory period during which no new inputs are allowed and the potential remains constant. To prevent strong negative polarization of the membrane, its potential is constrained to $u_{min} = u_{rest}$. As long as $u > u_{min}$, continuous leak of the membrane potential occurs.

Simulation details: The spiking-neuron dynamics and learning procedure were simulated using a custom Python implementation. The code included modules for Poisson rate-based image encoding, leaky-integrate-and-fire output-neuron dynamics, STDP-inspired synaptic weight updates, and reconstruction of the learned synaptic weight maps. The simulated network consisted of 16 input neurons and 2 output neurons, corresponding to the 16 pixels of the 4×4 input image and the two target diagonal-pattern classes, respectively. Each training pattern was presented for 22 ms with a numerical time step of 0.1 ms. The 22 ms window was chosen to provide enough presynaptic spike events for the active pixels, while the 0.1 ms step ensured stable integration of the LIF dynamics.

Initial synaptic weights were randomly sampled from a uniform distribution in the range [0.1, 0.3], corresponding to weak but non-zero initial connections that allow both output neurons to participate in the early competition. The LIF parameters were $R = 1$, $C = 1$, $u_{threshold} = 0.01$, $u_{rest} = 0$, and refractory time 0.2 ms. In normalized model units, R and C set the membrane time constant $\tau_m = RC$, the threshold controls the spike-generation condition, and the refractory time prevents immediate repeated firing of the same output neuron. Input spike trains were generated according to a Poisson process with firing probability proportional to the corresponding pixel intensity. The STDP-inspired update was applied within a temporal window of 5 simulation steps around the postsynaptic spike, which allowed the algorithm to identify presynaptic events temporally correlated with the output spike. The same numerical settings were used for all simulations shown in this section.

Since STDP is considered as an unsupervised learning method, we apply characteristics of competitive learning to our task to create competition between neurons in the output layer. From a biological point of view[65], the ability of an excited neuron to reduce the activity of its neighbors is known as lateral inhibition. By applying lateral inhibition, we create contrast in stimulation, which enhances sensory perception. This is quite similar to what we observe in the "winner-takes-all" (WTA) strategy in unsupervised machine learning methods. Here, the winner is the neuron that generates the first action potential in response to the input pattern. After generating the first spike, it suppresses the excitation of all other neurons in the output layer and fully adjusts its synaptic weights to the input pattern (see Figure 5). Choosing a fixed threshold value for all neurons creates a situation where one neuron dominates the response pattern and prevents the other neurons from participating in the reaction. To address this issue, we apply an adaptive threshold, in which the threshold value of a neuron increases each time it fires an action potential. We represent this adaptive threshold as $u_{threshold} + \theta$, where the threshold is increased by $\theta = 0.001$ each time the neuron fires. By adopting this adaptive threshold, the excited neuron requires more input impulses to fire again within a short period following the action potential, thus allowing other neurons to compete for subsequent input patterns.

The learning process in SNNs was implemented by sequentially presenting training patterns, each over a 22 ms time window (see Simulation details). Specifically, each pattern was randomly presented to the network input, thereby creating natural competition for each individual output neuron. As a result, each output neuron becomes more activated in response to a specific class, enhancing its specialization for that class. A significant distinction of such neural networks is the implementation of unsupervised learning in real-time, meaning that learning occurs during the network's operation. The selection of the initial weights followed a uniform distribution within the range [0.1, 0.3], which was selected based on the optimal balance between accuracy and learning speed. During the tracking of dynamics between the output and input layers, images of the weight coefficients for each output neuron were generated over the training time, where the pixel brightness reflected the strength of the connection between the corresponding output neuron and the input layer neurons.

The evolution of the synaptic weights was visualized by mapping the 16 input-to-output conductance values of each output neuron back onto the original 4×4 pixel grid. In these maps, brighter pixels correspond to stronger synaptic conductance and therefore to stronger coupling between the corresponding input pixel and the selected output neuron. This representation makes it possible to directly compare the target input pattern with the synaptic pattern learned by each output neuron during training. These maps represent the weights of the single fully connected synaptic layer connecting the 16 input pixels to the output neurons; the present architecture does not contain a convolutional layer.

As shown in Figure 7, the initially weak and randomly distributed synaptic weights gradually reorganize into two distinct spatial patterns. For the output neuron that wins the competition for the right-diagonal input, conductance increases primarily in synapses corresponding to pixels of the right diagonal. The same process occurs independently for the second output neuron, which becomes selective to the left-diagonal input. Therefore, classification is performed by comparing which output neuron reaches the firing threshold first for a given input spike pattern. The dynamics clearly demonstrates the learning speed in our model with appropriately chosen parameters: after a few hundred pattern presentations, each output neuron had learned its respective pattern, with no further significant changes in the weights. A key area of research in both classical neural networks and spiking neural networks is the challenge of determining the optimal initial weight distribution. This aspect is critical, as it directly impacts the speed and accuracy of model training. The emergence of noise during experimental weight training is attributed to the non-uniformity of potentiation and depression in the devices. However, the network retains its ability to recognize patterns despite this variability.

The binary classification task considered here was selected as a minimal proof-of-concept demonstration of device-assisted STDP-inspired learning. It is not intended as a benchmark of large-scale image-recognition performance. The same hardware-in-the-loop framework can be extended to multi-class classification by increasing the number of output neurons and active synaptic connections; however, the implementation and optimization of such a multi-class classifier are beyond the scope of the present study.

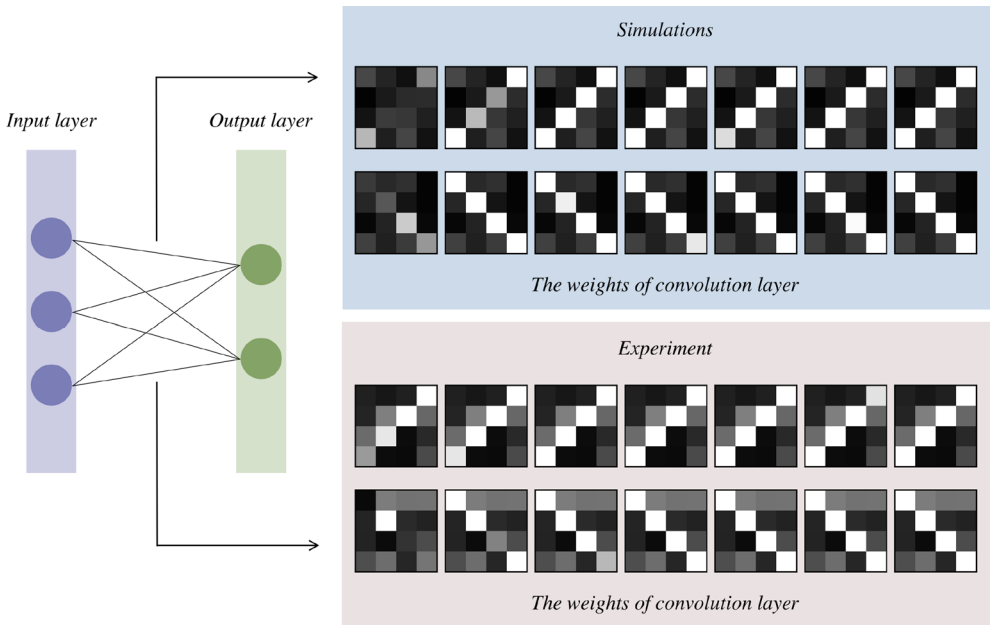


Fig. 7. Temporal evolution of the input-to-output synaptic weights during learning of two 4×4 diagonal patterns. Each 4×4 map represents the input-to-output synaptic weights of the single fully connected layer connecting the 16 input pixels to one output neuron; brighter pixels correspond to larger conductance values and therefore to stronger synaptic connections. The first output neuron becomes selective to the right-diagonal pattern, whereas the second output neuron becomes selective to the left-diagonal pattern. The upper panel shows the numerical simulation obtained using the same LIF neuron dynamics and STDP-inspired update rule, while the lower panel shows the result reconstructed from the experimentally measured conductance-response characteristics of the optoelectronic synapses.

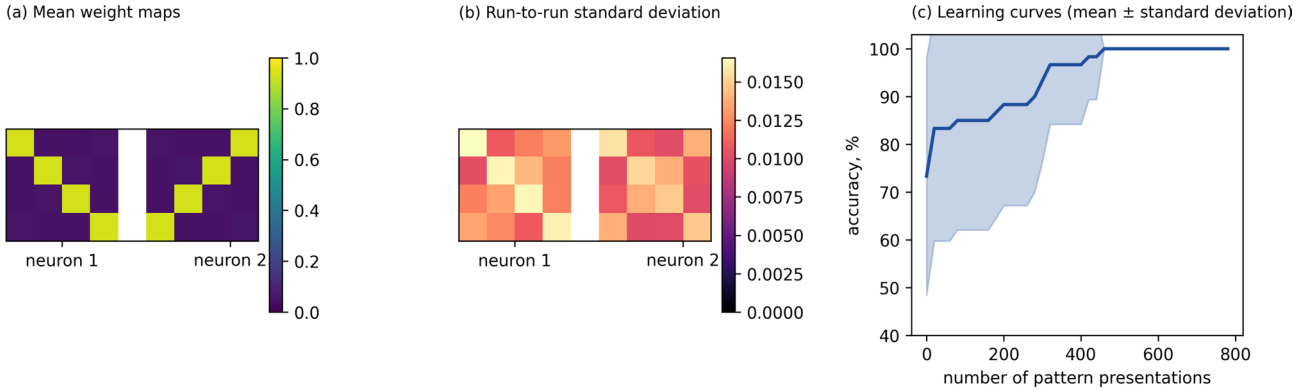


Fig. 8. Repeatability of the unsupervised learning in simulation, over 30 independent runs with different random initial weights (uniform [0.1, 0.3]) and Poisson spike-encoding seeds. (**a**) Mean final synaptic-weight maps of the two output neurons (left: neuron 1, right: neuron 2); the right- and left-diagonal patterns are reproduced consistently. (**b**) Pixel-wise run-to-run standard deviation of the final weights (standard deviation ≈ 0.013), concentrated on the active diagonal pixels. (**c**) Classification accuracy versus the number of pattern presentations (mean ± standard deviation over the 30 runs), showing a reproducible convergence to 100% accuracy. This analysis is based on simulations of the learning model.

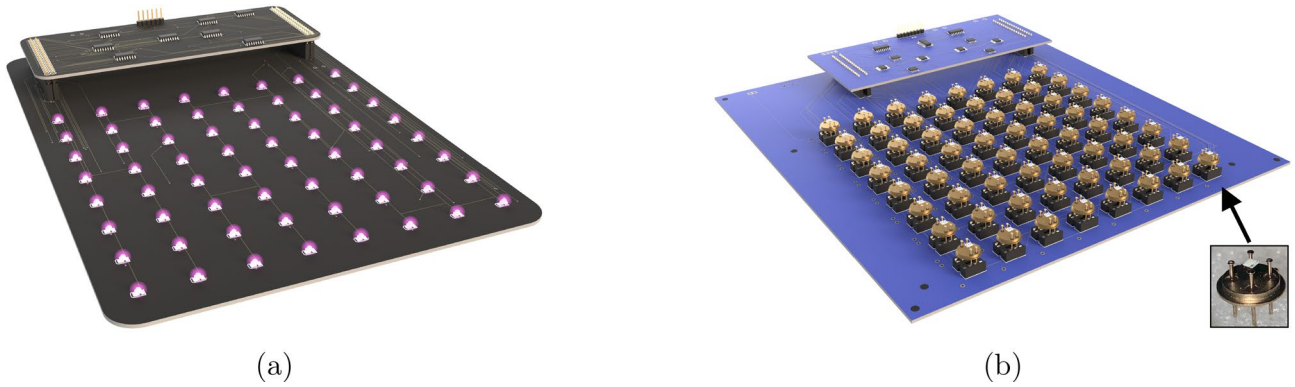


Fig. 9. (**a**) 3D view of the LED chip. (**b**) 3D view of the measurement chip with the devices placed on it.

To assess the robustness of the learning, we performed a repeatability analysis in simulation. The training was repeated over 30 independent runs with different random initial weights (uniform [0.1, 0.3]) and Poisson spike-encoding seeds. In each run, the two patterns were presented in randomly ordered cycles during training, and the classification accuracy was evaluated on independently generated, Poisson-encoded test presentations of the two patterns; for reference, a random, untrained network corresponds to chance level ($\approx 50\%$ on this binary task). The mean final synaptic-weight maps (Figure 8a) reproduce the two diagonal patterns, with output neuron 1 selective to the right diagonal and output neuron 2 to the left diagonal, while the pixel-wise run-to-run standard deviation (Figure 8b) is small (≈ 0.013) and concentrated on the active pixels. The classification accuracy converged to 100% in all runs along a reproducible learning trajectory (Figure 8c). We emphasize that this repeatability analysis is performed in simulation; a systematic experimental characterization of device-to-device variability across many physically distinct devices, together with long-term endurance, is identified as an important direction for future work.

We provide approximate energy and speed estimates for the present prototype, stating the underlying assumptions explicitly. The presynaptic optical event is dominated by the LED: for the operating irradiance of 3.2 mW/cm^2 at the device, a 1 s pulse, and an illuminated device area A, the delivered optical energy per pulse is $E_{\mathrm{opt}} = 3.2\ \mathrm{mW/cm^2} \times A \times 1\ \mathrm{s}$; for an assumed active area $A \approx 1\ \mathrm{mm^2}$ this gives $E_{\mathrm{opt}} \approx 30\ \mu\mathrm{J}$ per pulse. The electrical read-out dissipates a power $P = V^2/(R_s + R_{\mathrm{dev}})$ per device, so for a read window t_{read} the read energy is $E_{\mathrm{read}} = P\,t_{\mathrm{read}}$; for $V = 3.3$ V, an effective resistance in the 10^2–$10^5\ \Omega$ range, and $t_{\mathrm{read}} \approx 1$ ms, this gives roughly 10^{-7}–10^{-4} J per read-out, several orders of magnitude below the optical write energy. We stress that the low stimulation frequencies (0.01–0.5 Hz) used in the device characterization reflect the slow conductance-adaptation and relaxation timescales that govern learning, and are not a measure of inference speed: once the synaptic conductance state is established, classification is limited by the electrical read-out and multiplexing electronics rather than by the relaxation time. The optical write energy is currently dominated by

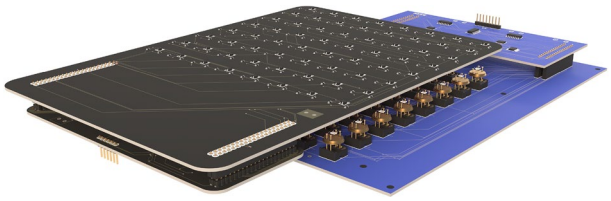


Fig. 10. 3D view of the experimental setup.

the discrete, off-chip LED and the large device area, and integrated micro-LED or waveguide-coupled sources would reduce it substantially.

The present 8×8 LED/device platform is a laboratory-scale proof-of-concept, and we discuss its scaling honestly. The system currently uses one discrete LED and one electrical read-out channel per synapse, and a 5 cm LED-to-device spacing was required to keep optical crosstalk from neighbouring emitters below the measurement noise; this spacing is not suitable for compact integration. Compact scaling will therefore require integrated, individually addressable optical sources (for example micro-LED arrays or waveguide-coupled emitters) together with parallel, multiplexed mixed-signal read-out. At the array level, the optical write scheme does offer a genuine and bounded advantage: because potentiation is induced optically and contactlessly, no programming current flows through unselected devices, so the write sneak-path and write-disturb problems of electrically programmed resistive crossbars are absent. Optical addressing also provides a natural high fan-out, since a single presynaptic optical source can illuminate many synapses in parallel without electrically loading the driving line. The electrical read-out, however, still requires current flow through the selected devices and therefore needs proper multiplexing and parasitic-current management in large arrays; for the resistance values used here this read current is small and does not appreciably perturb the stored conductance. We thus present optical writing as mitigating one of the two classic crossbar bottlenecks rather than as a complete solution to all array-level scaling problems.

To conclude, we have examined the applicability of metal oxide semiconductors in the context of neuromorphic applications. Synaptic plasticity response characteristics were obtained as a function of thermal exposure to control the forgetting time. A device-assisted, STDP-inspired learning method for image-pattern recognition was proposed and demonstrated in a hardware-in-the-loop configuration. Long-term endurance over many program/erase cycles, extended retention measurements, and integrated large-scale implementations are identified as important directions for future work.

Experimental section

Synthesis of nanocrystalline semiconducting metal oxide nanocrystallites films

The synthesis of nanocrystalline zinc oxide (ZnO) was carried out using a precipitation method from an aqueous solution of basic zinc carbonate, resulting from the reaction of zinc acetate ($Zn(CH_3COO)_2$) with ammonium bicarbonate (NH_4HCO_3), followed by thermal decomposition of the resulting $Zn_x(CO_3)_y(OH)_z$ at 300°C in air. The annealed nanocrystalline ZnO powder was then mixed with terpineol, and the resulting suspension was applied to the surface of a substrate made of aluminum oxide (Al_2O_3) with platinum (Pt) electrodes. The synthesis process of tungsten oxide (WO_3), tin oxide (SnO_2) and indium oxide (In_2O_3) is similar to the methods used for obtaining ZnO nanocrystals. The method has been described in more detail in Ref.[66].

Development of neuromorphic chip

To create a system of unified experimental synapses, a neuromorphic computational chip was developed for the demonstration and implementation of learning in spiking neural networks based on synaptic connections made from semiconductor metal nanocrystals. Light pulses generated by LED (SMD 0603, 395 nm) are used as the pre-neuron. Synthesized semiconductor metal oxides serve as the synapses. The computational system consists of a control chip for excitatory LEDs, which adjusts the conductivity of the device, and a chip for measuring the conductivity of the devices, with the ability to address and control each element of the system individually. These components are integrated into a unified system using a microcontroller, which is connected to a computer. The system is capable of integrating up to 64 synapses. A printed circuit PCB chip was developed for an array of LEDs arranged in an 8×8 matrix. This configuration provides 64 individually controllable LEDs. Figure ashows the LED board with the control chip mounted on top, which is connected to an ADC.

The second component of the neuromorphic computing chip is the measurement module, which is equipped with specialised platforms for the integration of the developed devices. Each element features an addressable control system that provides direct access to the parameter measuring process. The control modules and structural components are integrated with each other through contact connections located at the top of the PCB, as shown in Figure b. During the integration process of the two control chips, the optimal distance between the LEDs and their device was determined to be 5 cm, aiming to minimize undesirable parasitic light exposure from neighboring LEDs. The connection between the LEDs and the devices is shown in Figure 10.

Experimental setup

The individual circuit components had been assembled, they were integrated into a system in which each synaptic device was positioned beneath its own stimulating LED. For the training experiments, only a 4×4 array

of LEDs was activated, even though the system architecture is designed to accommodate a larger number of elements. Presynaptic spikes are synthesized digitally by the microcontroller and converted into optical pulses by constant-current LED drivers; postsynaptic electrical pulses (conductance changes) are read through a series resistor into the ADC and fed back to the controller for weight updates. The same control board handles the per-device normalization described above.

The functional roles of the hardware and software components are separated as follows. The optoelectronic metal-oxide devices serve as physical synapses whose conductance represents the synaptic weight. The LED control board generates optical presynaptic stimuli that modify the conductance of selected devices, while the measurement board and ADC provide electrical readout of the conductance states. The microcontroller synchronizes LED actuation, conductance readout, and data transfer to the host computer. The host computer performs the network-level calculations, including LIF membrane-potential integration, output-spike detection, lateral inhibition, and STDP-inspired update scheduling. Thus, the present system demonstrates physical synaptic plasticity embedded in an externally controlled hardware-in-the-loop learning loop.

Data availability

Data sets generated during the current study are available from the corresponding author on reasonable request.

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Author contributions

V.V. Krasnikov and A.A. Chezhegov performed the experiments and theory and analyzed the data. V.V. Krasnikov constructed the experimental setup with help from A.S. Chizhov. A.A. Grunin and A.A. Fedyanin supervised the project and interpretation of the data. V.V. Krasnikov wrote the manuscript with input from all authors. All authors reviewed the manuscript.

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Declarations

Competing interests

The authors declare no competing interests.

Additional information

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